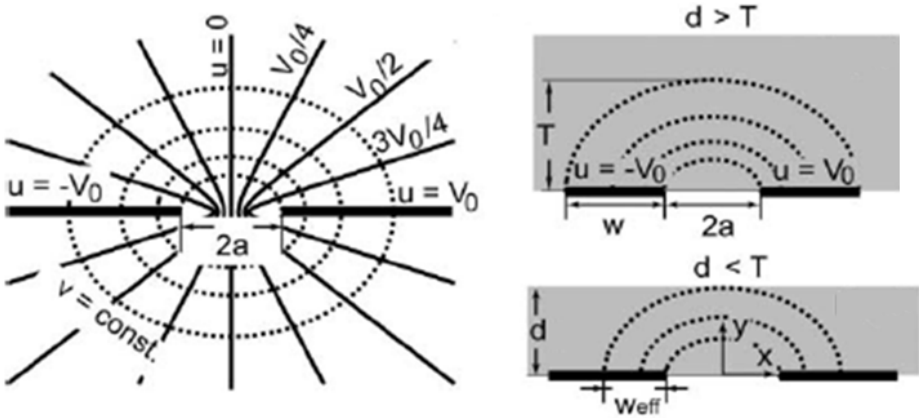
Parasitic Capacitance: Silicon Or Dielectric Substrates

Coplanar Electrodes On Dielectric Substrate



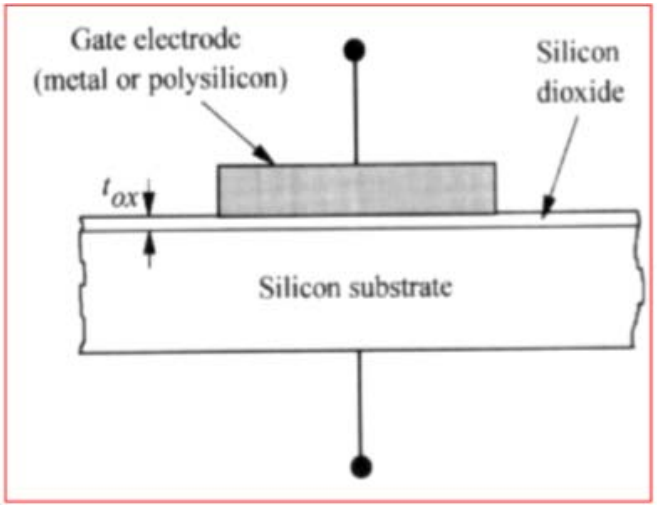
$$T = a \sinh\left[\cosh^{-1}\left(1+\frac{w}{a}\right)\right] = a\sqrt{\left(1+\frac{w}{a}\right)^2 - 1}$$

$$\frac{w_{eff}}{a} = \cosh\left[\sinh^{-1}\left(\frac{d}{a}\right)\right] - 1 = \sqrt{1+\left(\frac{d}{a}\right)^2} - 1$$

$$C = \frac{2\varepsilon_r\varepsilon_0}{\pi} L \ln\left[\left(1+\frac{w}{a}\right) + \sqrt{\left(1+\frac{w}{a}\right)^2 - 1}\right]$$

T is the electrical field penetration depth;
w_{eff} is the effective electrode width;
C is the capacitance between the electrodes.

Coplanar Electrodes On Semiconductor



$$\frac{1}{C_{MOS}} = \frac{1}{C_{ox}}\left(1 + \frac{2kT/e}{|V_g - V_s|}\right) \cong \frac{1}{C_{ox}}$$

$$C_{MOS}(depletion) = \frac{\varepsilon_{ox}}{d_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{SC}} W_{dep}} = \frac{C_{ox}}{\sqrt{1 + (2C_{ox}^2 V_g / \varepsilon_{SC} e N_A)}}$$

C_{ox} is the capacitance crossing the insulation layer, i.e. $\varepsilon_{ox}A/t_{ox}$.